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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/018,658	12/21/2001	Kunijuki Kajita	L9289.01227	2181

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STEVENS DAVIS MILLER & MOSHER, LLP
1615 L STREET, NW
SUITE 850
WASHINGTON, DC 20036

EXAMINER	
CHAUDRY, MUJTABA M	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 09/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/018,658	KAJITA, KUNIJUKI	
	Examiner	Art Unit	
	Mujtaba K Chaudry	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *34-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *34-51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06/03/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The corrected or substitute drawings were received on May 18, 2004. These drawings are accepted.

Specification

The corrected or substitute specification were received on May 18, 2004. The specification is accepted.

Response to Amendment

The Examiner hereby acknowledges Applicants' proposed cancellations of claims 1-33 and introduction of claims 34-51, which are essentially and amended form of previously submitted claims. Applicant's arguments/amendments with respect to cancelled claims 1-33 and newly added claims 34-51 filed June 3, 2004 have been fully considered but are not persuasive. The Examiner would also like to point out that this action is made final (See MPEP 706.07a).

Applicant contends, "...Kato fails to disclose or suggest a concatenating unit that concatenates the transport blocks having the CRC-bit..." The Examiner respectfully disagrees. The Examiner would like to analyze the term "concatenate." Concatenate is defined by the The Authoritative Dictionary of IEEE standards Terms 7th edition as:

"to append one item to the end of another so as to form a single unit in a contiguous pattern."

Kato teaches (Figures 4 and 5D) a packet assembly circuit which assembles packets in a concatenated format as defined above. FIGS. 5a-5d are schematic representations showing the operation of the hybrid FEC/ARQ communications system of the first embodiment, wherein FIG. 5a shows basic transmission data, FIG. 5b shows division of the basic transmission data into data packets; FIG. 5c shows addition of an error detecting code to each data segment; and **FIG. 5d shows creation of a data packet by addition of a packet header to each data segment complete with the error detecting code.** The data transmitter A comprises an input terminal 10, a packet assembly circuit 12, data memory 22, a transmit/receive circuit 24, and a retransmission request circuit 26, as shown in FIG. 4. **The packet assembly circuit 12 is comprised of a segmentation circuit 14, an error detecting code addition circuit 16, and a header addition circuit 20.** The input terminal 10 receives basic transmission data AD, as shown in FIG. 5A. The basic transmission data AD corresponds to a BCH code. More specifically, the basic transmission data AD is changed to the BCH code by appending a BCH-based parity code (BCHD), which acts as an error correcting parity code, to the basic data BD. An encoder 5 carries out the generation of the basic transmission data AD from the basic data BD. The segmentation circuit 14 divides the basic transmission data AD into a fixed length, as shown in FIG. 5b. The error detecting code addition circuit 16 appends an error detecting code to the thus-divided data segments, as shown in FIG. 5c. A CRC code is herein used as the error detecting code. The header addition circuit 20 further appends a packet header to each data segment complete with the CRC code, whereby a transmission data packet is generated, as shown in FIG. 5d. As described above, the packet assembly circuit 12 appends the error correcting code for ARQ purposes to the basic transmission data AD having subjected to FEC.

The data memory 22 stores the transmission data packet generated by the packet assembly circuit 12. The data memory 22 maintains the transmission data packet after having sent it to the receiving side. This is because it is possible for the data memory 22 to quickly retransmit the transmission data packet if it receives a retransmission request from the receiving side. The transmit/receive circuit 24 sends the transmission data packet stored in the data memory 22 to the data receiver B, as well as receiving a retransmission request from the data receiver B. Upon receipt of a retransmission request from the data receiver B via the transmit/receive circuit 24, the retransmission request circuit 26 causes the data packet that is the object of the retransmission request to be output to the transmit/receive circuit 24 from the data memory 22. The data receiver B is provided with a transmit/receive circuit 28, an error correcting circuit 30, and an error detecting circuit 32, as shown in FIG. 4. The transmit/receive circuit 28 receives data from the data transmitter A, as well as sending a retransmission request to the data transmitter A. The transmit/receive circuit 28 acts as a receiving circuit and a transmitting circuit. After having received all the basic transmission data AD divided into a plurality of data packets, the error correcting circuit 30 carries out an error correcting operation using the BCH code, as show in FIGS. 7a to 7c. There may be a case where errors arising in the packets can be corrected by the above-described error correcting operation. The error detecting circuit 32 detects errors in the data thus corrected by the error correcting circuit 30 using the CRC code, as shown in FIG. 7d. If errors are detected, a request for retransmission of the data packet found to contain errors will be sent to the data transmitter A via the transmit/receive circuit 28. Therefore, although Kato does not explicitly teach a concatenating unit, he clearly teaches the functionality of it according to the definition of the term concatenate.

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 34-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kato (USPN 5844918).

As per claims 34-36 and 46-48, Kato substantially teaches (title and abstract) an error correcting code including basic data and a BCH-based parity code appended thereto is divided into smaller packets. An error detecting code is appended to each of the thus-divided packets, so that transmission basic data is formed. When the transmission basic data is received, the basic data and a BCH-based parity code are derived from the transmission basic data. Error correcting is carried out with respect to the overall transmission basic data. An error detecting operation is carried out with respect to each packet using the error detecting code. If a packet is found to contain errors, a request for retransmission of that packet will be sent to the sending side. Kato teaches (col. 16, lines 39-67) a digital transmission method for sending a digital signal comprising: a division step of dividing an error correcting code which includes basic data and a parity code, into smaller data segments; an error detecting code addition step of appending an error detecting code to each of the data segments divided in the division step; a transmission step

of sending the data segments complete with the error detecting code on a packet-by-packet basis; and a retransmission step of retransmitting a requested data packet in response to a retransmission request of the data packet from a receiving side. This procedure in shown by example in Figure 5, wherein the input terminal 10 of the data transmitter A receives the basic transmission data AD (see FIG. 5A), and the received basic transmission data is sent to the packet assembly circuit 12. The basic transmission data AD has already been changed to a BCH code by addition of a BCH-based parity code to the basic data BD as a result of the FEC operation. The basic transmission data AD is divided into data segments by the segmentation circuit 14 of the packet assembly circuit 12 so that they can be assembled into packets, as shown in FIG. 5b. The error detecting code addition circuit 16 appends the CRC code to each data segment, as shown in FIG. 5c. The header addition circuit 20 appends a packet header to the data segment complete with the error detecting code, whereby a transmission data packet is assembled, as shown in FIG. 5d. The thus-assembled transmission data packet is stored in the data memory 22 and sent to the data receiver B via the transmit/receive circuit 24.

Kato does not explicitly teach a concatenating unit that concatenates each of the data blocks having the CRC as stated in the present application.

However, the Examiner would like to point out that Kato teaches in Figure 5B to divide the basic data, which is analogous to transport blocks of the present application. CRC is then appended to each of the data blocks. Although Kato does not explicitly teach to concatenate all of the CRC data blocks, he does show a data memory (Figure 4, Reference #44), which is used to store the transmitted packets in case of a request for retransmission. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to add a

concatenating unit to concatenate the CRC data blocks. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that by using a concatenating unit to concatenate the CRC data blocks would improve on packet synchronization during transmission.

As per claims 37-39 and 49-51, Kato substantially teaches, in view of above rejections, (Figure 5 and col. 9, lines 10-37) the input terminal 10 of the data transmitter A receives the basic transmission data AD (see FIG. 5A), and the thus-received basic transmission data is sent to the packet assembly circuit 12. The basic transmission data AD has already been changed to a BCH code by addition of a BCH-based parity code to the basic data BD as a result of the FEC operation. The basic transmission data AD is divided into data segments by the segmentation circuit 14 of the packet assembly circuit 12 so that they can be assembled into packets, as shown in FIG. 5b. The error detecting code addition circuit 16 appends the CRC code to each data segment, as shown in FIG. 5c. The header addition circuit 20 appends a packet header to the data segment complete with the error detecting code, whereby a transmission data packet is assembled, as shown in FIG. 5d. The Examiner would like to point out that at least one of the segmented data blocks in Figure 5D has less data than the other data blocks. Subsequently, the assembled transmission data packet is stored in the data memory 22 and sent to the data receiver B via the transmit/receive circuit 24. Kato also teaches (col. 16, lines 53-68) a digital transmission method for sending a digital signal, comprising: a division step of dividing an error correcting code which includes basic data and a parity code, into smaller data segments; an error detecting code addition step of appending an error detecting code to each of the data segments divided in the division step; a transmission step of sending the data segments complete with the

error detecting code on a packet-by-packet basis; and a retransmission step of retransmitting a requested data packet in response to a retransmission request of the data packet from a receiving side.

As per claims 40-45, Kato substantially teaches, in view of above rejections, (Figure 4) the system and method digital data transmission to be for a communications system which obviously encompasses a mobile station and a base station.

The Examiner disagrees with the Applicant and maintains rejections with respect to cancelled claims 1-33 and newly added claims 34-51. All arguments have been considered. It is the Examiner's conclusion that amended claims 34-51, which are essentially amended claims submitted previously, are not patentably distinct or non-obvious over the prior art of record.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing

date of this final action. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiries concerning this communication should be directed to the examiner, Mujtaba Chaudry who may be reached at 703-305-7755. The examiner may normally be reached Mon – Thur 7:30 am to 4:30 pm and every other Fri 8:00 am to 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Albert DeCady at 703-305-9595. The fax phone number for the organization where this application is assigned is 703-746-7239.

Any inquiry of general nature or relating to the status of this application or proceeding should be directed to the receptionist at 703-305-3900.

Mujtaba Chaudry
Art Unit 2133
September 22, 2004

GUY J. LAMARRE
PRIMARY EXAMINER